

Phase Frequency Detector with Adjustable Offset

Field of the Invention

The invention relates to phase frequency detectors and particularly to a phase
5 frequency detector in a phase lock loop (PLL) based frequency synthesiser.

Background to the Invention

Phase locked loops (PLL) are useful building tools available from several
manufacturers as a single integrated circuit. A typical PLL is shown in Figure 1 and
10 incorporates a phase frequency detector (100), a charge pump (110), a low pass filter element
(120) and a voltage controlled oscillator (VCO) (130). A clock signal Rclk is provided as a
first input to the phase detector (100) and a feedback signal, Nclk, the output of a frequency
divider, is provided as a second input. In this known phase locked loop, PLL, based
frequency synthesiser, the outputs of the tri-state phase/frequency detector, PFD (100), are
15 used to drive the charge pump (110).

Although shown as an integer- N PLL in Figure 1, such PLL's can be modified to
fractional -N by using an interpolator to control the frequency divider. The tri-state PFD has
particular application for fractional-N frequency fractional synthesis, as noisy digital activity
may be performed while the PFD is in it's off state. However, the use of the these PFD in
20 fractional -N phase detectors suffers from a problem associated with its non-linearity
behaviour around the origin. Other types of phase detectors (e.g. XOR based) do not suffer
from problems associated with non-linearity problems, but do have other problems that
obviate their effectiveness in use in these applications. If the problem of non-linearity could
be overcome the PFD would be the preferred detector for the fractional-N PLL application.

Figure 2 details the PFD (100) that can be used in the circuitry of Figure 1. It
comprises two D-type flip-flops (201, 202), the D input of both being tied to a logic high. A
reference frequency Rclk clocks a first flip-flop (201) and a signal frequency Nclk clocks the
second flip-flop (202). The outputs of both flip flops are input to an AND gate (203), the
output of which is the input to a delay element (204), the output of which is then input to the
25 reset input of both flip-flops (201, 202). It will be understood that both flip flops are therefore
provided with the same signal to their respective reset inputs. The effect of this input from the
AND gate (203) and delay element (204) ensures that the output of each flip-flop has a
minimum pulse width. The output of each flip-flops drives an individual charge pump (205,
206), the charge pumps being connected at a common node (207) that provides the output,

Icp, of the circuit, the output, Icp, being the combination of current from the first and second charge pumps.

The charge pump output, Icp, can have three states, “up” active, “down” active and “off”, the states being driven from the outputs of the flip-flops of the PFD. When “up” is active Icp sources current Iup (205). When “down” is active, Icp sinks current Idn (206).
 5 When neither pump-up (205) nor pump-down (206) is active, Icp is zero so the charge pump is in the “off” state. If Iup and Idn are perfectly matched then Icp is also zero when both pump-up and pump-down are active.

It will be understood therefore that the PFD/charge pump combination outputs a net
 10 pulse of source current, Iup, if the Nclk phase lags the Rclk phase, the pulse width being proportional to the phase difference between the two signals. Similarly, a net sink current pulse, Idn, is output if the Nclk phase leads the Rclk phase, again of width proportional to the phase error.

In any cycle, the presence of the delay element (204) ensures that both “up” and
 15 “down” outputs of the PFD circuitry are active for at least the period τ (known as the anti-backlash delay), before the flip-flops are reset. This ensures that there is no dead-zone in the phase detector when the phase error is very small. The anti-backlash delay is typically chosen to be at least as long as the turn-on time of the current sources. A timing diagram shown in Figure 3 illustrates an example where the Nclk phase leads the Rclk phase, i.e. the VCO
 20 output frequency is too high. The net result is that a negative current pulse, of width proportional to the input phase error, is output (Icp) from the charge pump which acts to slow down the VCO output frequency. When the PLL is in lock with small phase error, the tri-state charge pump is only on for the anti-backlash period, which is typically a small fraction of the reference period. This gives the tri-state PFD good immunity to substrate noise.

As seen in Figure 1, the output of this circuitry is low pass filtered (120) before
 25 driving the VCO (130), the frequency divided output of which is used as the feedback loop signal and the input Nclk to the second flip flop (202). The presence of a positive or negative pulse from the phase detection circuitry causes the VCO (130) to change frequency and phase until Rclk = Nclk in both frequency and phase. The output of the phase detection circuitry is
 30 therefore adopting a zero value and the VCO (130) is locked onto that frequency.

As discussed previously, the integer -N circuitry may be modified to form a fractional-N PLL, such as that shown in Figure 4. The same reference numerals are used for similar components. Such a circuit incorporates a fractional interpolator (401) to control the

N divider (402) in the feedback loop. Typically, an interpolator such as a sigma-delta modulator with an output containing a DC component equal to the interpolated fractional value and an error component high pass shaped versus frequency is used to effect a modulation of the phase of the Nclk edge at the PFD input in such a way that its average value is equal to the phase of reference input to the PFD, and with noise shaping in the modulator ensuring that quantised phase noise is shaped to have a high frequency characteristic which is subsequently attenuated by the low pass loop filter (120). A typical PFD/charge pump transfer function is shown in Figure 5. Positive output charge corresponds to net “up” current out of the charge pump, negative output charge corresponds to net “down” current. Mismatch between the “up” and “down” charge pump currents causes a non-linearity in the PFD/charge pump transfer function in the region of the zero input phase error point. This non-linearity generates harmonics of the shaped quantised phase noise signal on Nclk, which can alias down in-band when sub-sampled at the PFD reference rate. The aliased quantisation noise typically looks like discrete spurs at frequencies of multiples and sub-multiples of the reference frequency divided by the modulus of the interpolator. With dither added to the interpolator, the aliased frequencies spread out into finer frequency bins and looks more like broad-band noise, which results in degraded phase noise performance out of the synthesiser.

In order to obviate this problem it is possible to utilise a charge pump with sufficiently low mis-match so that the aliasing effect is negligible. Such a charge pump is however costly to make. An alternative solution is to add a fixed phase offset to the input phase error signal so that operation of the PFD and charge pump is biased away from the zero phase point, thus avoiding the non-linearity region.

The offset should be large enough to ensure that the Nclk edge modulates either the width of the “up” pulse OR the width of the “down” pulse and not ever both. When the Nclk edge location is modulated by the sigma-delta modulator, the offset should be greater than the largest phase deviation effected by the sigma-delta output from its average output value. For example, a suitable fractional interpolator such as a 3rd order MASH sigma-delta modulator generating interpolated fractional values between 0 and 1, outputs, once every clock cycle, one of eight integer values that can lie in the range -3 to +4 inclusive. This implies that the worse case deviation of an Nclk edge around its nominal edge location is within +/-4 RF clock cycles and hence an input phase offset in the PFD, that corresponds to 4 RF clock cycles should be sufficient.

The aforementioned PFD problem is specific to fractional-N PLL's. Prior art PFD structures tend to address additional problems and examples are described in Chapter 5 of *Frequency Synthesis By Phase Lock: William F Egan 2nd Edition Wiley Interscience* which refers to dead-zone and cross over problems that are characteristic of standard tri-state PFD architecture when operating close to the zero phase error point. If the phase detector's operating point moves into the dead-zone region the loop is effectively open and this results in a large increase in noise at the VCO output. Just out-side this dead-zone region the detector's gain response is highly non-linear. As the input error increases the detector's gain linearity improves as in this case the up or down pulses are wide enough to turn the current sources on to their final value, producing a net output charge proportional to the input phase error.

A widely used solution to the dead-zone problem is to insert a delay, t , in the reset path to both flip-flops as shown in Fig. 2. This is what is shown in Fig. 2 and its operation has been described above. The key idea here is to ensure that, near zero phase difference, both current source outputs are produced rather than neither. This always produces an output response, which is the difference between the up and down current pulses.

This solution for eliminating the dead-zone works well for an Integer-N PLL where monotonicity rather than linearity in the phase detector transfer function is sufficient to maintain low noise performance. Up/down current mismatch does, however, cause reference spur side-bands to appear around the PLL output frequency. In an Integer-N PLL the reference may only be a decade above the loop bandwidth and thus reference spurs will see limited attenuation by the low pass loop filter response. Reference spurs are much less of an issue in a fractional-N synthesizer as the much higher offset reference spurs are greatly attenuated by the loop. However, the non-linearity due to mismatch poses a problem specific to fractional-N, particularly when a high order noise shaping based fractional interpolator is used. The non-linearity causes harmonic distortion of the noise shaped phase signal on the Nclk input to the PFD and these harmonic distortion products can alias down inside the loop bandwidth due to the sub-sampling operation of the PFD.

Egan describes alternative solutions other than inserting the anti-backlash delay element, to the deadzone and cross over distortion problem. One of these is the use of a constant bleed current, such as that shown in Figure 6, as a solution to the crossover distortion problem. This works on the principle that, when the PFD is inside a PLL, the feedback loop acts to bring the average phase detector output to zero, hence a phase offset

will be produced at the input to the PFD so that an appropriate opposite polarity pulse of current is output to cancel, on average, the charge due to the constant bleed current. Thus, steady state operation of the phase detector in the PLL is biased away from the zero phase error point, thus avoiding the cross-over distortion problems.

5 While the average or DC output of the detector is zero, the constant bleed along with the regular pulse of correction current will produce an AC error signal at the detector output. This AC signal will have a strong fundamental component at the reference frequency and lower magnitude components at harmonics of the reference frequency all of which will produce FM spur side-bands at the PLL output. The strong fundamental component produced
10 by this constant bleed method is the most troublesome as this gets the least attenuation from the loop filter.

Egan further refers to US Patent 4,970,475 of Gillig the disclosure of which is incorporated herein by way of reference and which describes a pulsed bleed solution to the cross-over distortion problem which works in a similar way to the constant bleed solution,
15 but with a reduced spur component at the reference fundamental frequency. An example of such a circuit is shown in Figure 3 of Gillig. In this circuit two flip flops are provided, the inputs to both flip flops being tied to a logic high. The first flip flop is clocked with a reference signal whereas the second flip flop is clocked with a variable frequency feedback signal. The outputs of the flip flops are ANDed and the resulting AND gate output delayed by
20 a delay element. The output of the delay element is then used to reset one of the flip flops while the output of the AND gate prior to the delay element is used to reset the other flip flop. Each of the flip flop outputs is used to enable a charge pump- a negative polarity source and a positive polarity source, the output of the circuit being the common node between the two charge pumps. The circuit maintains a lock condition in a phase locked loop by extending the
25 DOWN pulse enabling the negative polarity charge pump to the same width as the UP pulse that enables the positive pump; thereby creating a net zero charge.

Alternative embodiments to the solution addressed by Gillig are shown in Figs 6, 7 and 9 (also shown in Fig. 5.36 of Egan) of his Patent by introducing an equal delay in the path controlling the correcting current. This additional delay causes the correcting pulse to
30 overlap with the bleed pulse in time so that the residual output is minimised, thus reducing the reference spur component further. This is a significant improvement in an integer- N PLL but is much less so in a fractional- N PLL. This is because in the fractional -N PLL, the

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residual spurs in the illustrated example of Figure 3 of Gillig tend to be already sufficiently attenuated by the loop.

As well as being solutions to the dead-zone and cross over distortion problems, as described by Egan, this input phase offset produced by either the constant bleed or the pulsed bleed implementation of Gillig provides a way to avoid the up/down mismatch non-linearity that causes aliased in-band noise in a fractional-N PLL. If the phase offset is larger than the peak phase deviation on the Nclk edge, then the Nclk edge modulates either the up or down current pulse width, but not both. The constant bleed current method carries additional broad-band noise and the fact that it is on over the complete reference cycle means that it is susceptible to noise and interference pick-up.

Of particular concern, specific to a fractional-N synthesizer, is noise coupling from the fractional interpolator circuitry when it is on the same substrate as the charge pump circuit. While the noise shaped output of the interpolator has a spectrum with little energy inside the loop bandwidth, the digital switching activity internally in the interpolator has significant energy in its spectrum at frequencies lower than the PLL bandwidth. Substrate noise arising from switching activity at these frequencies couples through to the charge pump while Icp is on, resulting in noise side-bands appearing around the carrier at offsets equal to the noise frequency. Hence, it will be appreciated that the always on bleed current solution, while reducing the level of aliased spurs, can increase the overall in-band noise and spur level due to substrate coupling. The inherent noise produced by the bleed current device also adds to the in-band noise.

The implementation of Fig. 3 of Gillig is an improvement on constant bleed because the pulsed bleed current source is only active for a fraction of a reference cycle which means it's broad-band noise contribution will be lower. However, because the reset to the reference flip-flop is delayed, the PLL will act to force the phase of Fv (or Nclk) to lead the reference (or Rclk). The implication of this is that the potential for interference from the interpolator, (the activity of which is triggered from the Nclk edge), getting into the charge pump is maximised. This hazard is illustrated in the timing diagram of Figure 7.

There is therefore a requirement for a device that provides an alternative solution to the the problems addressed by the bleed current and the Gillig solutions, and which does not substantially effect an incrementation of noise within the circuitry.

Summary of the Invention

These shortcomings of the prior art, and others, are addressed by the phase detection apparatus of the present invention. The provision of a delay element adapted to extend the trailing edge of the output of the flip flop being clocked with the feedback signal addresses the problem of overcoming the non-linearity problem. Furthermore, which is particularly important for fractional -N phase detection apparatus, the delay of the trailing edge of the feedback clocked flip flop relative to the reference clocked flip flop, moves the activity of the interpolator away from the charge pump activity, thereby reducing any cross-talk noise, when the apparatus is operating inside a PLL.

In accordance with one embodiment of the present invention, a phase detection apparatus or device for generating a phase difference signal for use in a phase lock loop (PLL) is provided. The apparatus has a first input for a reference signal, a second input for a loop feedback signal and outputs for the phase difference signal, and comprises a first storage element having a first clock input, a reset input and an output, and a second storage element having a second clock input, a reset input and an output. A logic element for logically combining the outputs of the first and second storage elements is provided, and has inputs coupled to the outputs of the two storage elements and an output. A delay element is coupled to the output of the logic element, the delay element having an output connected to the reset element of the second storage element. The reference signal is input to the first storage element and the loop feedback signal is input to the second storage element, the provision of the delay at the reset input to the second storage element effects a delay of the output of the second storage element with regard to the output of the first storage element.

In a preferred embodiment a second delay element coupled to the output of the logic element is provided. The second delay element has an output coupled to the reset element of the first storage element and the delay introduced by the second delay element to the first storage element is less than the delay introduced by the first delay element to the second storage element.

In an alternative embodiment the second delay element is coupled between the logic element and the first delay element, the output of the second delay element being coupled to the reset element of the first flip flop and the input of the first delay element.

Desirably, the logic element comprises a logic AND gate.

The two storage elements are preferably flip flops, and more preferably D type flip flops and further comprise data inputs coupled to a logic high.

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The output of the first storage element and the output of the second storage element are desirably coupled by a first current source having an enable input coupled to the output of the first storage element and a second current source having an enable input coupled to the output of the second storage element, the first and second current sources being coupled to form the output for the phase difference signal.

Preferably, the phase detection apparatus is a tri-state phase frequency detector.

In preferred embodiments, the delay element introduces a delay in the trailing edge of the second storage element relative to the trailing edge of the first storage element, the delay desirably being programmable.

Desirably, the delay is at least greater than the maximum deviation of the phase of the second storage element clock input.

In an alternative embodiment, the invention provides a phase detection apparatus also comprising: a first storage element having a clock input, a reset input and an output, and a second storage element having a clock input, a reset input and an output. Similarly to the first embodiment, a logic element for logically combining the outputs of the first and second storage element is provided, the logic element having inputs coupled to the outputs of the two storage elements and an output. In this embodiment, however, a stretching element for effecting a stretching of the trailing edge of the output of one of the first and second storage elements is provided, the provision of the stretching element effecting a stretching of the trailing edge of the output of one of the first and second storage elements, such that when used in a PLL, a compensating phase offset is introduced at the PFD input by the loop.

This embodiment may additionally comprise a delay element coupled to the output of the logic element, the delay element having an output coupled to the reset element of the second storage element.

The output of the delay element is optionally further coupled to the reset element of the first storage element.

The stretching element for effecting a stretching of the trailing edge of the output of one of the first and second storage elements desirably stretches the trailing edge output of the first storage element relative to the trailing edge output of the second storage element.

Optionally, the stretching element stretches the trailing edge output of the second storage element relative to trailing edge output of the first storage element.

In one embodiment the stretching element is located at the output of the first storage element. In another embodiment it is located at the output of the second storage element.

The phase offset is desirably a delay in the trailing edge of the output of the second storage element relative to the first storage element, and more desirably is programmable.

Typically, the delay is at least greater than the maximum deviation of the phase of the second storage element clock input.

5 The invention also provides a phase lock loop apparatus having a reference signal input and an oscillator output, the apparatus comprising: a filter element having an input and an output, controllable oscillator means having an input coupled to the output of the filter element and an output adapted to produce the oscillator output, a frequency dividing device having a first input coupled to the output of the oscillator output and an output for producing
10 a feedback loop signal, and a phase detection apparatus as hereinbefore described.

Further objects, features and advantages of the present invention will become apparent from the following description and drawings.

Brief Description of the Drawings

15 Figure 1 shows a known Integer-N Phase locked loop (PLL),
Figure 2 shows a known tri-state phase frequency detector (PFD) and charge pump for use with the PLL of Figure 1,
Figure 3 shows the operation of the PFD and charge pump of Figure 2 with perfectly matched up and down currents,
20 Figure 4 shows a known Fractional-N PLL,
Figure 5 shows a PFD transfer function with non-linearity due to mis-match,
Figure 6 shows a known PFD/charge pump with bleed current,
Figure 7 shows a time sequence associated with an alternative prior art solution with a time delay introduced to the Rclk flip-flop,
25 Figure 8 shows a PFD with phase offset means according to a first embodiment of the present invention,
Figure 9 shows the operation of a PFD/ charge pump combination according to the embodiment of Figure 8,
Figure 10 shows a PFD with a phase offset means according to a second embodiment of the
30 present invention,
Figure 11 shows a PFD with a phase offset means according to a third embodiment of the present invention,
Figure 12 is a timing sequence showing the operation of the device of Figure 11.

Figure 13 shows a PFD with an up output pulse stretch circuit,
 Figure 14 is a detail of the pulse stretch circuit of Figure 13, and
 Figure 15 shows a PFD with a down output pulse stretch circuit.

5 Detailed Description of the Drawings

Figures 1 to 7 have been hereinbefore described with reference to the prior art. Figure 8 shows a PFD with phase offset according to a first embodiment of the present invention for use with an interpolator circuit, which illustrates a way of introducing a phase offset at the PFD input by incorporating different “anti-backlash” delays for the up and down flip flops in the PDF. The same reference numerals are used for similar components. Similarly to that described with reference to the prior art circuits, the output of the two flip flops (201, 202) is presented as an input to the AND gate. In this embodiment the present invention differs from the prior art in that the output of the AND gate is then input to two different delay elements (801, 802). The output from each delay element is then input to the reset elements of the two flip flops. It will be appreciated that each flip flop is therefore provided with a different input to its reset element.

The timing diagrams in Figure 9 show an example where τ_2 is set greater than τ_1 . Since the loop acts to bring the average value of I_{cp} to zero, the time difference between the delays, $\tau_1 - \tau_2$, corresponds to the phase offset that will be introduced at the PFD inputs in closed loop. Therefore, in order to ensure that only either up or down current pulse is modulated by the interpolator, a phase offset corresponding to the peak deviation of the interpolated phase on N_{clk} is introduced at the PFD to ensure that the interpolator only modulates up current pulse widths. This delay of N_{clk} relative to R_{clk} is important for fractional-N PLL applications as the N_{clk} edge initiates the period of noisy digital activity in the interpolator circuit of the fractional - N synthesizer. The introduction of a lag on the N_{clk} edge relative to the R_{clk} edge offsets this activity away from periods during which the charge pump is active, thereby minimising substrate noise coupling.

It will be appreciated that the device of the present invention stretches the trailing edge of the “down” signal as shown in Fig. 9 (compared to Fig. 3). This results in the extra pulse of current as shown and thus extra charge to the LPF. The feedback loop acts to make the PFD/charge pump output, I_{cp} , to zero on average. This forces the “up” leading edge to advance by the same amount that the “down” falling edge is delayed.

Figure 10 shows an alternative circuitry adapted to effect the introduction of a phase lag at the second flip flop. In this embodiment only one delay element (1100) is introduced after the AND gate. The output of the delay element (1100) is input to the reset element of the second flip flop, and no delay element is introduced between the AND gate output and the reset element of the first flip flop. As such the overall effect is the same as that implemented using the circuitry of Figure 8, i.e. a time lag is introduced at the second flip flop relative to the first flip flop. Assuming that the up and dn outputs are zero, so as to effect an output current I_{cp} as zero, the leading edge of Rclk will cause a low to high transition on “dn”. When both “up” and “dn” are high the output of the AND gate will go high, resetting the “up” signal to low. A time τ later, the “dn” signal will reset to low. The timing sequence illustrated in Figure 9 is equally applicable for this embodiment, the effect on the PLL circuitry being that loop settles into a steady state with an average phase lag on Nclk’s rising edge relative to Rclk being equivalent to the amount of the delay introduced in the Nclk flip flop’s reset path.

By inserting the delay in the reset path to the Nclk flip flop the loop is forced to delay the Nclk edge relative to the Rclk edge and thus minimises the time that the activity of the interpolator overlaps with the charge pump activity.

It is also possible to achieve this effect of offsetting the activity of the interpolator away from the charge pump activity by utilising two delay elements as shown in Figure 11. A common delay (801) is implemented after the AND gate, and is followed by a further delay (802) on the reset of the Nclk flip flop. The first delay (801) could represent a finite delay from R to Q of real flip flops as well as the delay through the AND gate. The finite delay element results in an altered timing sequence, as shown in Figure 12, wherein there is an overlap of time when both the “up” and “dn” pulses are active.

In accordance with an alternate embodiment of the present invention, an alternative way of introducing a phase offset at the PFD input is effected by a stretching of the trailing edge of one of the PFD outputs relative to the trailing edge of the other output by incorporating a pulse stretch circuit (1300) as shown in the example in Figure 13. The charge offset at the output is given by the charge pump current times the extra amount the pulse is stretched. The loop tries to cancel error currents due to the output offset by introducing an equal and opposite offset between the PFD inputs.

For positive pulses, the pulse stretch circuit can be implemented as shown in Figure 14. When the input goes high the mn1 turns on, quickly discharging C1. Node n1 is pulled to ground and out goes high. On the trailing edge, when the input transitions from high to low, mn1 is turned off and n1 ramps up as C1 is charged up by the current source, p1. When n1 reaches V_T the trip point of the inverter, the output then goes low. The time for the output to go low after the input has gone low is given by

$$t = C.V_T / I \quad (\text{EQ 1})$$

The current I can be programmable to optimise the delay across different RF bands, with the optimum delay being just greater than the peak deviation of the interpolated phase on Nclk.

The timing diagram for the circuit of Figure 14 is similar to those shown in the example in Figure 9 result with $\tau_2 = \tau$ and the time difference, $\tau_1 - \tau_2$, generated by the pulse stretch circuit. As before, the loop acts to cancel error current due to this output offset by introducing an equal and opposite offset between the PFD inputs.

It will be appreciated that although described with reference to a positive pulse that a negative pulse may also be applicable, depending on the application. The utilisation on the down current enable is particularly applicable for fractional -N applications where the incorporation of the pulse stretch circuit on the “dn” signal path, as shown in Figure 15 ensures that in closed loop, Nclk will lag Rclk.

The solution provided by present invention is superior to the prior art bleed current method because the phase offset is created using a short pulse (<4 RF cycles typically) of offset current. It can be arranged to gate this on at a time when there is minimal digital activity in the sigma-delta modulator and thus minimal substrate noise. It offers advantages over that disclosed in Gillig in that there is minimal overlap in the operation of the interpolator with the activity of the charge pump.

The words “comprises/comprising” and the words “having/including” when used herein with reference to the present invention are used to specify the presence of stated features, integers, steps or components but does not preclude the presence or addition of one or more other features, integers, steps, components or groups thereof.

There has been hereinbefore described a phase detection apparatus which is improved over the prior art. It will be appreciated by those skilled in the art that modifications may be made without departing from the spirit and scope of the invention. Accordingly, it is not intended to limit the invention to any one described embodiment as it
5 will be appreciated by those skilled in the art that the invention should only be limited in view of the appended claims.

What is claimed is:

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T05420, 2753860